Designing Power Supplies Using Intersil's XDCP Mixed Signal Products

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Abstract

The objective of this Application Note is to illustrate the use of a Intersil XDCP® (Digitally Controlled Potentiometer) in the design of switching power supply. A mixed signal XDCP device is used to set the output voltage, the PWM (Pulse Width Modulation) frequency, and the over-current limit in a reference design of a *12V@10A* power supply. The techniques reflected in this working reference design could be used in the general power supply design for industrial, consumer, and communication systems.

A digitally controlled or electronic potentiometer overcomes many of the problems of its mechanical counterpart. The silicon, CMOS XDCP device has high reliability, no wiper movement due to environment, digital or computer controls, and a 'set and forget' calibration mode done manually or using automatic test equipment.

I. THEORY OF OPERATION

Digitally Controlled Potentiometer

The Intersil XDCP device is a potentiometer whose wiper position is computer or digitally controlled. The XDCP device also has memory where wiper settings and/or data can be stored. It is an analog-digital or mixed-signal, system level control device performing a component level function.

The block diagram of a typical XDCP IC is shown in Figure 1. The analog potentiometer is a variable three-terminal, resistive-like device whose wiper is controlled using one of three different serial buses. An example is the 3-wire bus. The control signals for the 3-wire bus are Up/Down (U/$\overline{D}$), Increment ($\overline{INC}$), and Device or Chip Select ($\overline{CS}$). The U/$\overline{D}$ input establishes the direction of the wiper, the $\overline{INC}$ input advances the wiper, and the $\overline{CS}$ input enables the device. One common way of using the potentiometer is as a programmable voltage divider.

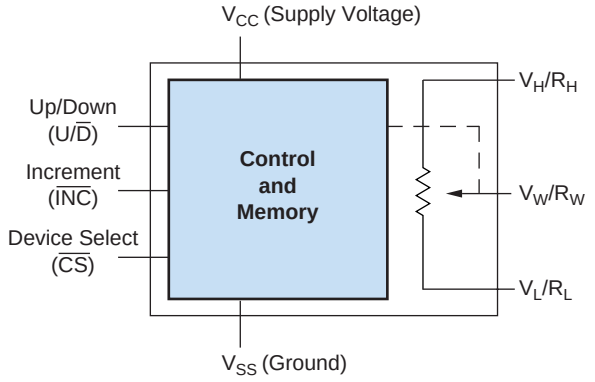


FIGURE 1. DIGITALLY CONTROLLED POTENTIOMETER

Switching Power Supply

This section provides an overview of the reference power supply design. It serves as a platform to understand the operation at the component level as described in the *Detailed Circuit Description, Section II*.

The reference design accepts either a 120Vac or 240Vac (switch selectable), 47Hz to 63Hz input power and delivers a regulated 12Vdc at 10A. The input voltage range is 100Vac to 132Vac or 200Vac to 264Vac. The output is a constant 12Vdc over the output current range of 0.5A to 10A. A minimum load of 0.5A is necessary for proper operation. Overcurrent protection will limit the output current to just over 10A.

Front End

Refer to the Block Diagram in Figure 2. AC input line, neutral and ground are connected to the Front End terminals L, N and G respectively. The Front End includes fuse protection, EMI filtering, input surge protection, rectification, AC input voltage range switch selection and DC capacitive energy storage and filtering. The Front End output is an unregulated nominal 320Vdc. The Front End output serves as the input to the Power Mesh.

Power Mesh

The Power Mesh consists of a DC/DC converter which converts the unregulated nominal 320Vdc to the 12Vdc output power. The DC/DC converter provides AC input to DC output isolation to address safety agency (e.g. UL) issues and 12Vdc output regulation. The topology is a conventional single switch forward converter using peak current control (PCC) to derive pulse width modulation (PWM) for the converter switch. The converter frequency is 110kHz with the frequency set point controlled by a Intersil XDCP IC located in the Primary Control. Power Mesh inputs from the Primary Control are primary bias (nominally 14Vdc) and PWM gate drive for the MOSFET switch. The Power Mesh provides a MOSFET current sense signal to the Primary Control. The Power Mesh generates the 12Vdc output and provides output voltage sensing to the Secondary Control.

Secondary Control

The Secondary Control contains a 2.5V reference and error amplifier. The error amplifier compares the reference voltage to a sample of the 12V output voltage. The amplified difference signal from the error amplifier output (error voltage) drives the LED of an optocoupler. The phototransistor in the optocoupler is located in the Primary Control. The optocoupler serves as an isolated feedback path for the error voltage. Also contained in the Secondary Control is a Intersil Digitally Controlled Potentiometer circuit. The XDCP circuit is used to calibrate the set point of the 12V output.

Primary Control

The Primary Control contains a UC3844A current mode PWM controller. This controller contains a PWM comparator. The voltage at the comparator inputs is derived from the primary switch current sense signal and the error voltage signal feed back from the Secondary Control via the optocoupler. The PWM comparator provides a PWM MOSFET gate drive to the Power Mesh. The pulse width defines a primary switch current, and hence the 12V output current, such that the 12V output voltage is held constant. An internal voltage clamp limits the primary switch current to a maximum value. This serves as an output overcurrent limit. A Intersil XDCP circuit calibrates this overcurrent limit. The UC3844A contains an R/C oscillator which determines the converter frequency. A second Intersil XDCP circuit is used to calibrate the set point of this oscillator such that the converter frequency is set accurately to 110kHz.

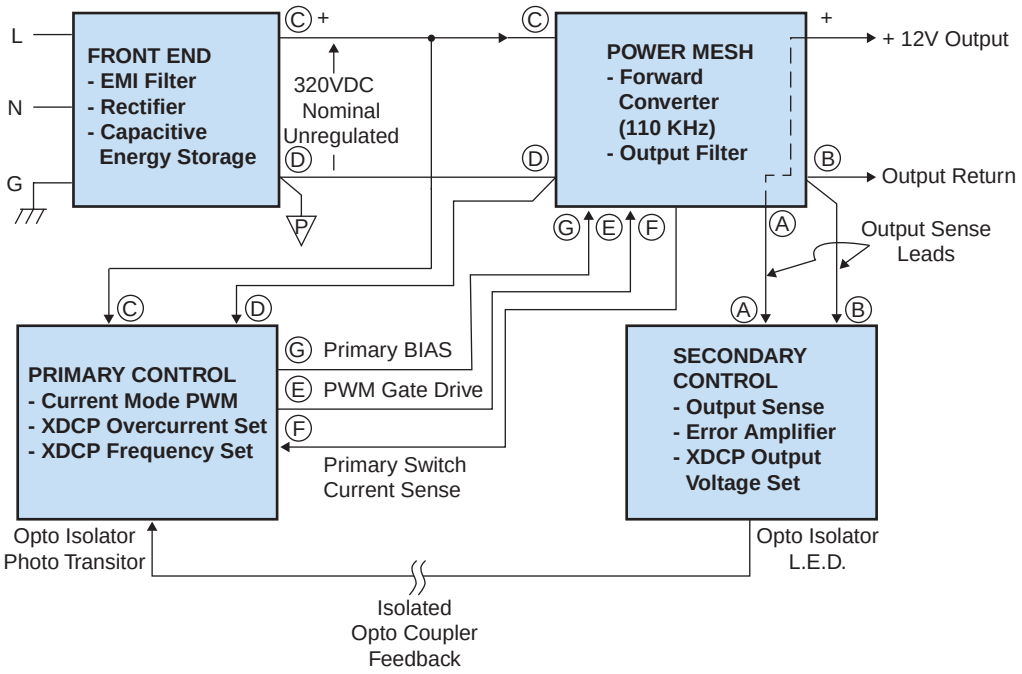


FIGURE 2. BLOCK DIAGRAM

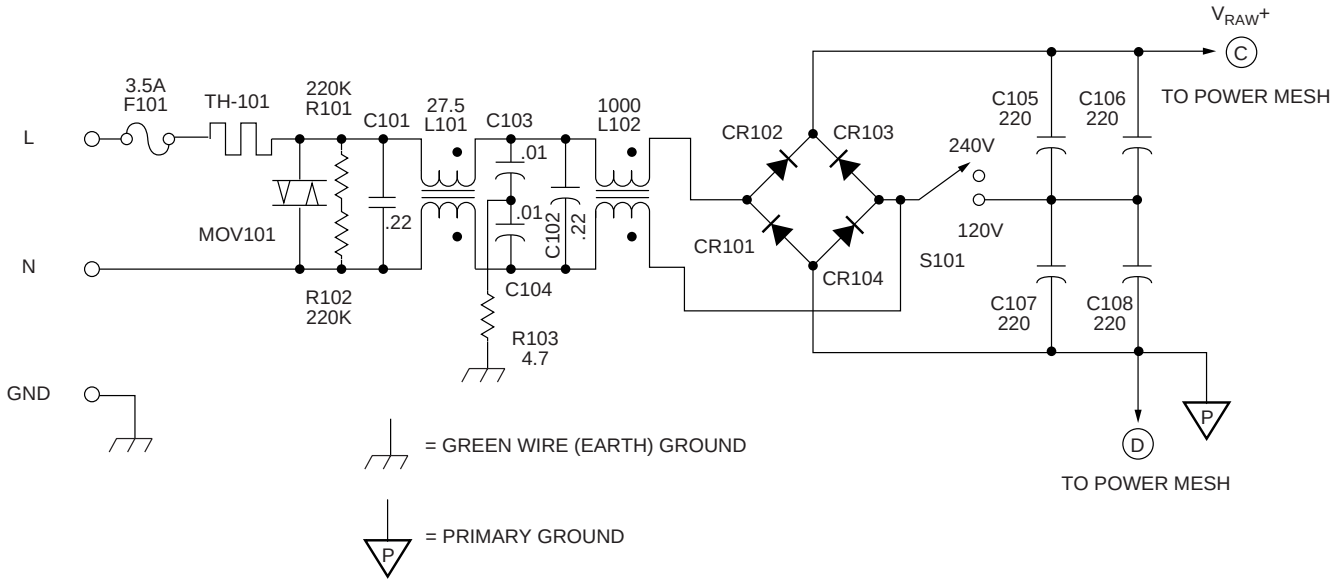


FIGURE 3. FRONT END

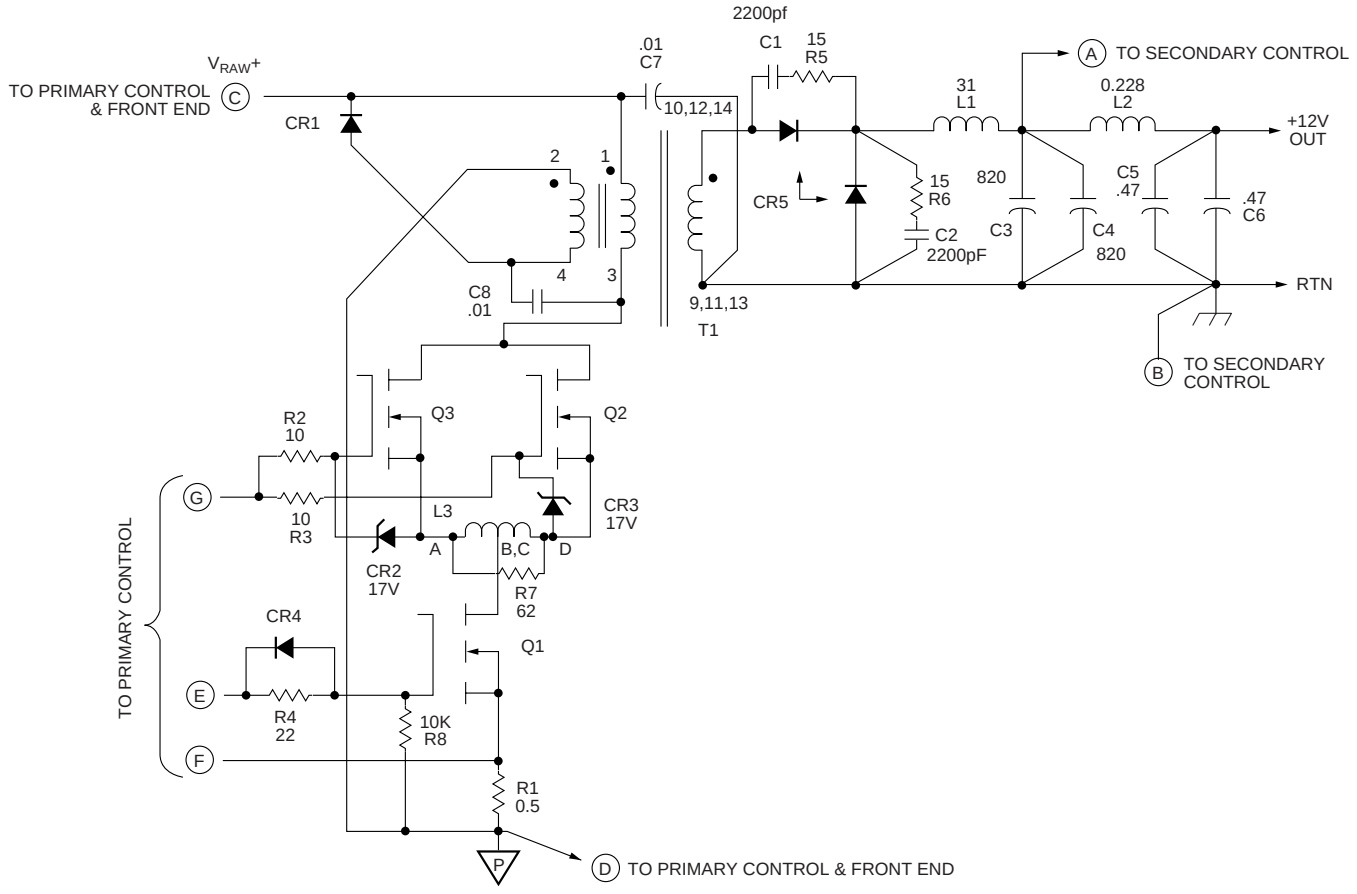


FIGURE 4. POWER MESH

II. DETAILED CIRCUIT DESCRIPTION

There are four circuit schematics: Front End (Fig. 3), Power Mesh (Fig. 4), Secondary Control (Fig. 5) and Primary Control (Fig. 6). The schematic interconnections are indicated by the circled letters on each schematic. These same circled letters also appear on the Block Diagram (Fig. 2) which illustrates these interconnections.

Front End

The Front End (Fig.3) processes AC line power and delivers an unregulated 320Vdc to the down stream DC/DC converter in the Power Mesh (Fig.4).

Referring to the Front End (Fig.3) schematic, F101 provides protection in the event of a failure which draws excessive AC line current. F101 is chosen to have an adequate time delay characteristic such that input surge current will not blow the fuse.

TH101 is a negative temperature coefficient thermistor. When cold (input power is initially applied), the thermistor resistance is high enough to limit the inrush current. When hot, after the power supply is running for a few seconds, the thermistor resistance drops to a low value to minimize dissipation.

C101 and C102 are across-the-line safety agency rated X capacitors which function to attenuate differential mode conducted EMI. R101 and R102 are bleeder resistors to discharge C101 and C102 quickly in the event the power supply is unplugged from the AC line thereby exposing the line cord plug pins. These bleeder resistors reduce a potential shock hazard.

L102 is a common mode inductor which provides significant impedance to common mode EMI. Most of the common mode EMI current which does flow through L101 is shunted to ground via C103 and C104. These capacitors are safety agency rated line-to-ground Y capacitors. Resistor R103 prevents C103/C104 and parisitic inductance from forming a high Q resonant circuit which could cause an unwanted peak in the common mode noise spectrum. L102 also has a leakage inductance between the two winding which serves as an impedance for differential mode conducted noise. L101 functions in a similar manner to L102 except it is a much smaller value and serves to attenuate high frequency EMI.

MOV101 is a metal oxide varistor which clamps high voltage power line spikes to reduce the probability of damage to down stream circuitry. With S101 in the 240V position, rectifiers

CR101-CR104 act as a full wave bridge. From the positive end of C105 to the negative end of C107, the capacitor bank is charged to the peak of the nominal 240Vac input voltage. With S101 in the 120V position CR102 charges C105 and C106 to the positive peak of the nominal 120Vac input voltage whereas CR101 charges C107 and C108 to the negative peak. Thus for either 120Vac or 240Vac operation the voltage across the capacitor bank is a nominal 320Vdc. This voltage is unregulated, contains considerable 2X power line frequency ripple and may have an instantaneous value ranging from 200V to a maximum of 373V.

Power Mesh

Refer to Figure 4. The power mesh is a DC/DC converter which processes nominal 320Vdc power from the Front End and delivers a regulated 12Vdc at 10A to the output.

The topology is known as a single switch forward converter. The switching frequency was chosen to be 110kHz and trimmed accurately by a Intersil digitally controlled potentiometer in the Primary Control. This insures that the 4th harmonic of the switching frequency will always fall below the 450kHz lower frequency limit of the FCC conducted EMI requirement despite manufacturing component tolerances. As low order EMI component amplitudes roll off at the reciprocal of harmonic frequency, this feature results in a 20% reduction in the value of the main EMI inductor, L102, in the Front End. The switch function is performed by transistors Q1, Q2, Q3 and associated components. The three transistors are connected in a cascode arrangement.

Q2 and Q3, 900V devices, operate in parallel as the top element of the cascode. Q2 and Q3 gates are held at a relatively constant 14Vdc, the primary bias voltage.

Q2 and Q3 source current is switched by Q1. Resistors R2 and R3 damp any parasitic inductance/gate input capacitance resonance to avoid gate voltage ringing. CR2 and CR3 are 17V Zener diodes to limit Q2 and Q3 gate to source voltage to a safe value under dynamic conditions. L3 is a center tapped inductor which tends to force Q2 and Q3 currents to be equal during the switching intervals to balance switching losses between Q2 and Q3. R7 across L7 serves to damp parasitic ringing. Q1 is switched OFF and ON, via R4 and CR4, by the PWM drive from the Primary Control. R4 damps Q1 gate voltage ringing during turn ON whereas CR4 allows rapid turn OFF. R8 insures Q1 is OFF in the absence of gate drive. As Q1 must only support the maximum source voltage of Q2 and Q3, it is a 60V device with a low Rds(on). The ON resistance of Q1 is a small fraction of that of Q2 and Q3 so the bulk of the Rds(on) losses and switching losses occur in Q2 and Q3. Q1 requires no heat sink whereas Q2 and Q3 must have a heatsink to dissipate a bit under 2W each. The advantage of this cascode switch scheme is that the gate charge required to switch Q1 is small compared to that required to switch Q2 and Q3. Thus Q1 can be driven directly from the Primary Control PWM chip, UC3844A, without the component count and time delay associated with high current drive circuitry.

R1 is a current sample resistor. T1 primary current flowing to primary ground through the switch develops a voltage across R1. This voltage serves as the current sense voltage for the UC3844A control chip in the Primary Control.

T1 is the converter transformer. With the switch ON, 320V nominal Vraw is imposed across T1 primary winding (terminals 1 and 3). T1 clamp winding (terminals 2 and 4) has the same turns as the primary. With the switch ON, T1 terminal 4 is driven to minus Vraw thus CR1 is reversed biased. When the switch is turned OFF, T1 exciting current and leakage inductance energy causes T1 terminal 3, and hence terminal 4 voltage to rapidly rise. When terminal 4 reaches Vraw, CR1 conducts and clamps terminal 4 to Vraw. By transformer action this clamps terminal 3 to twice Vraw. Because of a small amount of leakage inductance between T1 primary and clamp winding, terminal 3 clamping is imperfect. C8 serves to bypass this leakage inductance and enhance the clamping of terminal 3 thus controlling the maximum voltage stress on Q2 and Q3

T1 secondary (terminals 9,11,13 and 10,12,14) provide output power to the secondary rectifier CR5. The secondary is appropriately insulated from the primary to address safety agency isolation issues. CR5 is a dual Schottky rectifier to minimize rectification losses. Nonetheless, CR5 heatsink must be sized to adequately dissipate about 7 Watts. C1/R5 and C2/R6 serve as output rectifier snubbers.

L1 is the main output inductor which feeds the output capacitors C3 and C4. L2, C5 and C6 provide high frequency spike filtering. The node of L1, L2, C3 and C4 is chosen as the output voltage sense point to avoid including the L2, C5 and C6 double pole in the output voltage control loop.

C7 serves to short circuit common mode noise generated via T1 primary to secondary capacitance. C7 is located close to T1 thereby making this EMI current loop physically small to minimize magnetic field radiation. This substantially reduces the common mode noise voltage which must be attenuated by the Front End EMI filter.

As C1 spans the primary to secondary isolation barrier, C1 must be a safety agency rated Y capacitor.

There is an additional winding on T1 that is not shown on the Power Mesh schematic. This winding, terminals 6 and 7, provides primary bias and is shown on the Primary Control schematic (Fig.6).

Secondary Control

The Secondary Control (Fig.5) is powered by the12V output and contains the output voltage reference, error amplifier and Intersil XDCP device for setting the output voltage.

U203 is a TL431A which contains an internal 2.5V reference and high gain error amplifier. The non-inverting amplifier input is internally connected to the 2.5V internal reference (see Fig.8). The inverting amplifier input is connected to the node of R203 and R204. These resistors serve as the output voltage divider. The output of the TL431A error amplifier is connected to R202. R202 converts the error amplifier output voltage into a current to drive the LED in optocoupler U204. R201 insures zero LED current when the U203 error amplifier output is high but U203 still draws a small bias current. C202 and R209 determine the transfer function of the error amplifier to achieve overall voltage feedback loop stability.

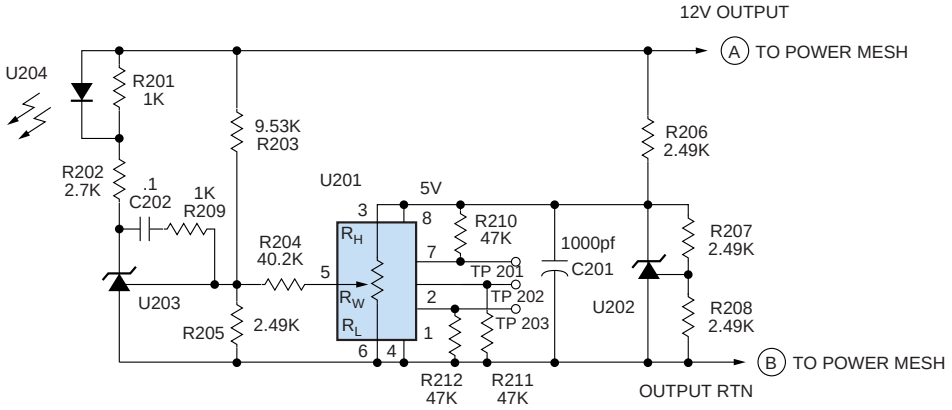


FIGURE 5. SECONDARY CONTROL

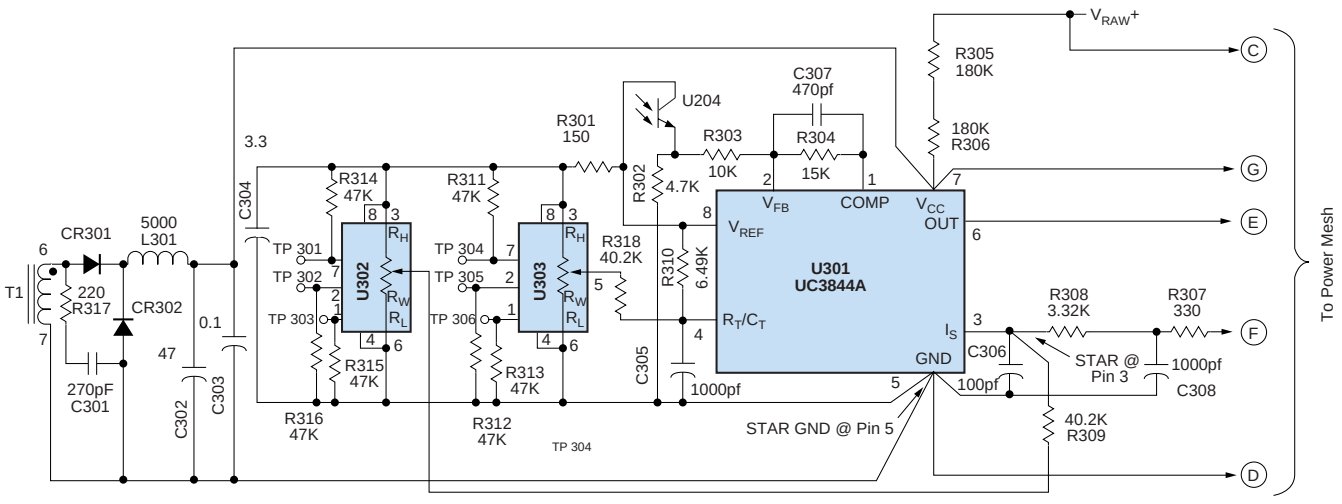


FIGURE 6. PRIMARY CONTROL

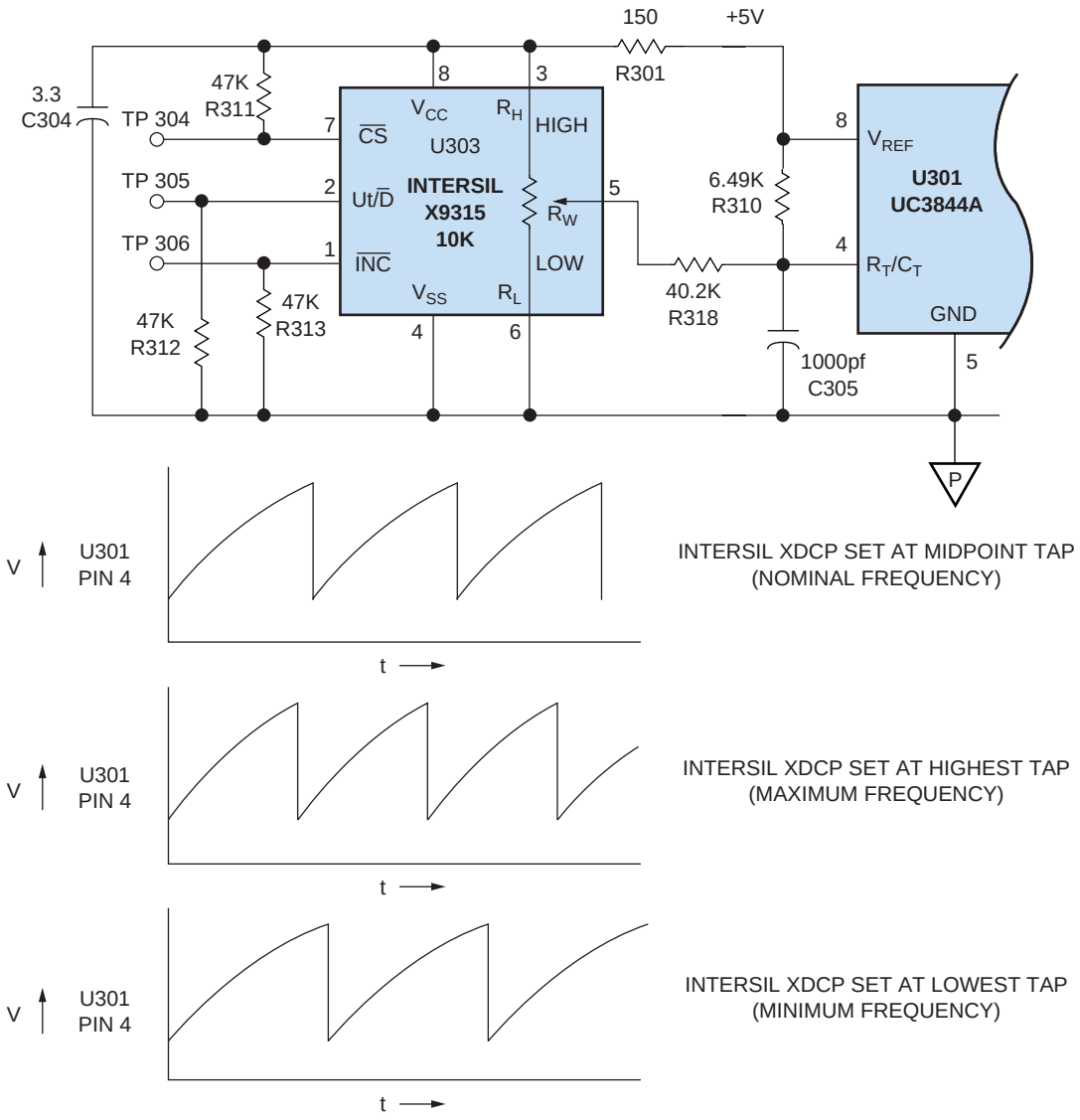


FIGURE 7. XDCP CONVERTOR FREQUENCY CONTROL

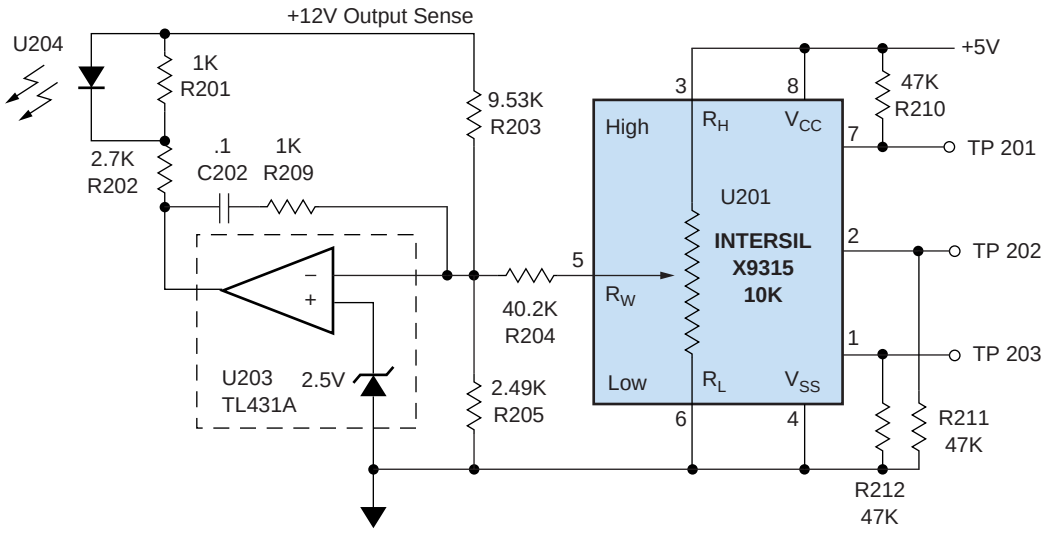


FIGURE 8. XDCP OUTPUT VOLTAGE CONTROL

Setting the Output Voltage

Output voltage trim, Figures 5 and 8, is achieved with U201, a X9315, 10kΩ digitally controlled potentiometer. R204 connects the XDCP wiper to the U203 summing junction (R203, R204, R205 node). When the XDCP wiper is at the bottom of the 10k XDCP resistor (OUTPUT RTN), current flows out of U203 summing junction through R204. This causes the U203 error amplifier to increase the +12V output such that the current through R203 is increased by an amount equal to the R204 current. By a similar mechanism, raising the XDCP wiper to +5V end of the XDCP 10kΩ resistor lowers the +12V output. This XDCP circuit is capable of trimming the nominal output voltage ± 0.6V. As the X9315 is a 32 tap device, the output voltage can be set in approximately 40mV increments. Other components in Figure 5 function to provide the +5V power supply for the XDCP circuit. R207 and R208 form a 2:1 voltage divider causing the cathode terminal of U202, a TL431A, to maintain a constant +5V. R206 supplies bias current for U202 and U201. C201 serves as a noise bypass. TP-201, TP-202 and TP-203 are XDCP test points to allow programming of the IC. R210, R211 and R212 ensure that the XDCP wiper position remains fixed when the device is not being programmed. U201 pin 7 is the NOT chip select input, normally held high by R210. Pin 2 is the up/NOT down input normally held low by R211. Pin 1 is the NOT increment input normally held low by R212.

Primary Control

Refer to the Primary Control schematic (Fig.6). The Primary Control is designed around U301, the popular, low cost, UC3844A PWM current mode controller. Start up bias for U301 is provided from Vraw through R305 and R306. U301 has a start threshold of 16V nominal and draws no more than 1/2mA before pin 7 is raised to the 16V start up threshold. When input power is applied, Vraw charges C302 via R305 and R306. When the voltage at U301 pin 7 reaches 16V nominal, U301 becomes active causing Vref, pin 8, to jump to 5V and pin 6 to deliver PWM to the Power Mesh switch. When U301 becomes active it draws about 20mA. U301 current is initially supplied from stored charge in C302. U301 will continue to run in the active mode until C302 voltage falls to approximately 10V, the low line lockout threshold of U301. However, before C302 voltage can fall to 10V, the Power Mesh begins operating causing converter transformer T1, pins 6 and 7 recharge C302 to maintain a nominal 14V bias on U301. R317 and C301 serve as a snubber network for bias rectifiers CR301 and CR302. L301 is the bias supply integrating inductor which provides current to C302. C303 is a high frequency noise bypass for U301.

Setting the PWM Frequency

The U301 clock frequency is determined, Figures 6 and 7, by R310, C305, R318 and the Intersil XDCP device U303. Figure 7 illustrates how U303 is used to trim the U301 oscillator frequency. Note that because U301 is a 50% duty cycle limited device, the U301 clock runs at twice the Power Mesh converter frequency. R311, R312 and R313 hold U303 programming pins to inactive levels when U303 is not being programmed. TP304, TP305 and TP306 are test points used for programming the wiper position of U303.

Output voltage feedback from the Secondary Control is coupled to the Primary Control by optoisolater U204. The phototransistor portion of U204 is shown in Figure 6. U204 collector is connected to 5V, the Vref pin (pin 8) of U301. R302 is connected from U204 emitter to primary GND (U301, pin 5). U204 phototransistor and R302 form a voltage divider. Depending on the U204 collector current, the

U204/R302 node will vary between 5V and GND. The U204/R302 node voltage serves as the input to an amplifier internal to U301. The inverting input of this amplifier is U301, pin 2. The non-inverting amplifier input is connected to a 2.5V reference within U301 (not shown). This connection is not available on a U301 pin. The amplifier output is U301, pin 1. Amplifier input resistor, R303 and feedback resistor R304 configure this amplifier for a voltage gain of 1.5. C307 serves to limit amplifier bandwidth to reduce high frequency noise on the amplifier output (U301, pin 1).

Internal to U301, there is a PWM comparator. The circuit in the upper right of Figure 9 illustrates this comparator. With the comparator output low, U301 pin 6 is low forcing the Power Mesh switch OFF. With the comparator output high, the power Mesh switch is ON. The comparator has a latching feature such that if the comparator inputs dictate the comparator output to be low, the output remains latched low until the latch is reset. Latch reset occurs on every other falling edge of the converter frequency clock waveform in Figure 7.

U301, pin 6, delivers a series of pulses to control the Power Mesh switch (see Fig. 9). The frequency of these pulses is the fixed converter frequency which in this design is 110kHz. The width of these pulses is modulated by the output voltage control loop. If the sensed output voltage is too low, pulse width is increased to raise the output voltage and visa-versa. Thus the output voltage is held constant by control of the PWM by the output voltage feedback loop. Key to achieving this PWM is the U301 PWM comparator.

The U301 PWM comparator has an inverting and non-inverting inputs as shown in Figure 9. The non-inverting input is fed from the U301 amplifier output, U301 pin 1 in Figure 6. Pin 1 is fed through two forward biased diode junctions, then to a 3:1 voltage divider (all internal to U301) and then to the non-inverting input of the PWM comparator. Thus the voltage at the non-inverting PWM comparator input is a bit less than 1/3 of the voltage on U301, pin 1. The voltage at the PWM comparator non-inverting input is clamped to a maximum or 1V by a U301 internal Zener diode as shown in Figure 9. If you trace the PWM comparator non-inverting input signal back to the Secondary Control error amplifier (U203 in Figures 5 and 8), this PWM comparator input can be thought of as direct function of the output of the Secondary Control error amplifier.

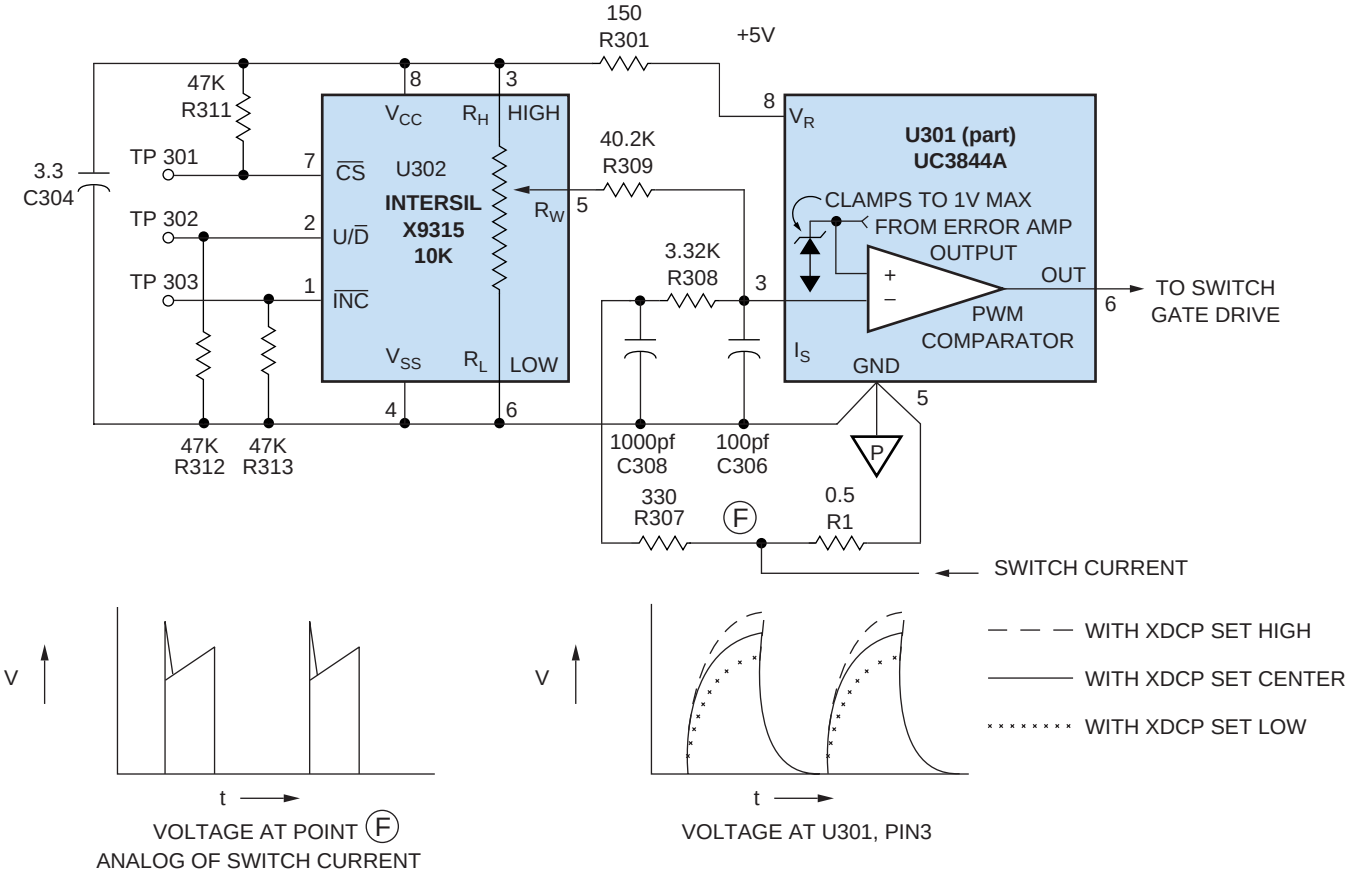


FIGURE 9. XDCP OUTPUT OVERCURRENT CONTROL

The PWM comparator inverting input is a voltage proportional to the 12V output current. Referring to Figure 4, 12V output current flows in T1 secondary winding (T1 terminals 9, 11, 13 and 10, 12, 14) when the switch is ON. Thus T1 primary (T1 terminals 1 and 2) current and switch current, which are the same value and are related to the 12V output current by the T1 turns ratio. T1 primary current flows through R1 to generate a voltage across R1 proportional to 12V output current. Returning to Figure 9, this voltage appears at the node of R1 and R307 and has a waveform shown in the lower left of Figure 9. The lead edge spike is due to charging of circuit capacitances at switch turn ON. The positive slope ramp following the lead edge spike is due to the current ramping up in T1 primary inductance and in the output inductor L1, of Figure 4, when the switch is ON. The Figure 9, R1/R307 node voltage is fed to the PWM comparator inverting input (U301, pin 3) through two cascaded integrators formed by R307/C308 and R308/C306. These integrators attenuate the lead edge spike on the voltage across R1. The waveform at U301, pin 3 is illustrated by the solid line in the lower right of Figure 9. Thus the two PWM comparator inputs are a voltage proportional to the output of the 12V error amplifier and a voltage proportional to the 12V output current.

The rising edge of the U301, pin 6 pulse occurs when the PWM comparator latch is reset at the falling edge of every other converter frequency clock pulse. The falling edge of the U301, pin 6 pulse occurs when the inverting PWM comparator input (voltage proportional to the T1 primary current) becomes higher than the non-inverting input (voltage proportional to the 12V error amplifier output) thereby setting the PWM comparator latch. Thus the 12V feedback loop, via the PWM comparator, maintains a constant 12V output by forcing the output current to an appropriate value such that the output voltage is held constant. If the inverting PWM comparator input does not set the PWM comparator latch, the latch will automatically be set by the falling edge of the next clock pulse. This limits the switch ON duty cycle to 50%.

Setting the Overcurrent Limit

The maximum output current over current limit is provided, Figures 6 and 9, by the U301 internal 1V Zener diode connected to the non-inverting input of the PWM comparator shown in Figure 9. This Zener limits the maximum voltage applied to the non-inverting input and hence the maximum voltage the inverting input can attain before the switch ON pulse is terminated. Since the inverting input voltage is proportional to 12V output current, this mechanism limits the 12V output current. Typically this current limit has a wide tolerance. The 1V Zener 10% tolerance plus the tolerance of all the other components which convert the 12V output current value to the PWM comparator inverting input voltage result in a situation where the worst case 12V overcurrent limit can be uncomfortably high. 1.5X or more of the maximum 12V output current is not uncommon. This forces the designer to insure that the Power Mesh components can handle these stresses along with the associated component cost. To alleviate this situation, a X9315 is used to trim out the tolerances associated with the overcurrent set point. U302, a Intersil X9315 10kOhm XDCP device is connected to the PWM comparator inverting input via R309. R309 injects a current into U301, pin 3 which is dependent on the XDCP wiper setting. With the wiper set high, the voltage at U301, pin 3 is increased as shown in the Figure 9 in the lower left dashed waveform.

This has the effect of reducing the 12V overcurrent limit. With the XDCP wiper set low, the 12V over current limit is increased. R301 and C304 provide a controlled rate of rise of U302 Vcc at turn ON. When U301 becomes active and U301, pin 8 jumps to 5V. It is essential to control the rate of rise of U203 Vcc at turn ON such that it complies with the Intersil X9315 data sheet. Resistors R311, R312 and R313 in Figure 9 hold the XDCP programming pins to inactive levels. TP301, TP302 and TP303 are test points to provide access to the XDCP programming pins. This overcurrent programming scheme can set the overcurrent trip point to 5% greater than the rated output current. Once the overcurrent point is reached, further reducing the power supply output load resistance will result in the output voltage falling. There will be the normal slight increase in output current when this occurs. Referring to the Primary Control schematic (Fig. 6), the U301 bias voltage across C302 decreases as the output voltage decreases. When the output voltage has fallen a few volts, the U301 bias voltage falls to the U301 low line lockout threshold (approximately 10V) causing U301 to become inactive. This stops the PWM drive and the 12V output voltage drops to zero. Automatic restart occurs when C302 is recharged to 16V by R305 and R306. Upon restart, normal operation is restored unless the output overload remains. If the overload remains, the power supply operates briefly in overcurrent limit mode until C302 is discharged to 10V causing U301 to once again become inactive. Restart attempts will continue until 12V output overload is removed. There is a relationship between the overcurrent limit point and the input AC line voltage. The overcurrent limit point increases a bit with increasing line voltage. In this design the 120V AC overcurrent trip point occurs at a 12V output current of 10.67A. This varies from 10.36A at 100Vac to 10.84A at 132Vac. The designer can achieve a first order compensation for this variation if so desired by connecting a high value resistor from U301, pin 3, to Vraw and resetting the values of R1, R308, R307, C306, C308 and R309 appropriately. The details of this are beyond the scope of this application note.

Parameter	Conditions	Test Data
Load Regulation:	0.5A to 10A (0.5A is minimum load), 120Vac	25mV (ΔV_{OUT})
Line Regulation:	100Vac-132Vac, 60Hz, 10A load	2mV (ΔV_{OUT})
Input Power:	10A load, 120Vac, 60Hz input	139W
Efficiency:	10A load, 120Vac, 60Hz input	86%
Output Voltage:	10A load, 120Vac, 60Hz input	11.985Vdc
XDCP Programmable Output Voltage Range:		11.394Vdc to 12.558Vdc
Converter Frequency:		109.6kHz
XDCP Programmable Converter Frequency Range:		101.7kHz to 122.9kHz
Onset of Overcurrent Protection:	120Vac, 60Hz input	10.67A
XDCP Programmable Overcurrent Protection Onset:		8.09A to 13.85A
Output Ripple & Noise:	10A load, 120Vac, 60Hz input, 20mHz Bandwidth	<100mV P-P

FIGURE 10. PERFORMANCE DATA

Performance Data for the Reference Design

The performance data for the reference design is tabulated in Figure 10. Note that the converter frequency was set via the XDCP converter to 109.6kHz, well within 0.5% of the target value of 110kHz. The converter frequency is XDCP programmable over the range of 101.7kHz to 122.9kHz. This is a total range of 21.2kHz. As the Intersil X9315 is a 32 tap device, programmable frequency increments are approximately 3% of the total range or 636Hz. There is a trade off between achieving the largest programmable range and the smallest programming increment. Referring to Figure 7, R318 (connected to the U303 XDCP wiper) can be changed to accommodate a different programming range. Increasing R318 reduces the programming range and decreasing R318 increases the range. But in all cases, the minimum adjustment increment is approximately 3% of the range with a 32 wiper tap device such as the Intersil X9315. The above comments relative to the programming of the converter frequency apply also to programming of the output voltage and overcurrent protection onset.

Should the power supply designer require smaller programming increments, Intersil offers other XDCP products with a greater number of wiper taps.

III. OTHER XDCP POWER SUPPLY APPLICATIONS

A digitally controlled potentiometer can be used in any application requiring electronic control of a potentiometer setting to adjust circuit parameters. Some suggested examples are:

1. Automatic calibration during production test is possible. A “bed-of nails” interface, similar to that used for parametric testing, provides a low cost access to the XDCP programming pins. Automating the calibration process reduces labor cost and improves product uniformity.
2. The power supply customer can be given control over certain parameters. For example, output voltage adjustment for margin testing can be easily programmed by the customer and offer far more options for adjustment than the conventional approach.
3. If optimizing dynamic response is a requirement, the XDCP programmability can be used to compensate for the wide initial tolerance of the feedback optocoupler current transfer ratio. Typically this tolerance is plus or minus 50% which forces the designer to reduce bandwidth by an octave to accommodate this tolerance.
4. For laboratory type power supplies, the XDCP device can replace front panel mechanical potentiometers. Not only does this offer the advantages of cost and reliability, but allows computer control of the front panel adjustments. Power supplies used in automatic test equipment can avoid the cost of A/D converters.

Intersil XDCP devices offer a reliable alternative to the mechanical potentiometer, plus it offers the advantage of electronically controlled adjustment.

IV. APPENDIX

Parts List and Magnetics Documentation

Bill of Materials/Parts List

POWER MESH

CODE	MFG	PART NUMBER	DESCRIPTION
CR1	MOT	MUR1100E	1A, 75ns, 1000PIV
CR2, CR3	MOT, PHA, FSC	1N5247	Zener, 17V, 500mW
CR4	MOT, PHA, NSC	1N4148	
CR5	IRF	IR30CPQ060	Dual Schottky 30A, 60V
Q1	IRF	IRFZ14	MOSFET 100V
Q2, Q3	IRF	IRFBE30	MOSFET 900V
C1, C2	Panasonic	ECU-S2A222KBA	2200pF, 5%, 100V, X7R
C3, C4	Panasonic	EEU-FCIC821S	820µF, 16V, FC Series
C5, C6	AVX	SR215E474MAA	.47µF, 50V, 25V, Ceramic
C7	Panasonic	ECQ-U2A103MF	.01µF/250V, Y- Capacitor
C8			0.01µF, 20%, 1000V, Z5u Ceramic
L1			Output Inductor, XIC-001, 31mH
L2			High Frequency Inductor, XIC-004, 0.28uH
L3			Balance Inductor, XIC-005
R1			0.5Ω, 1/2W
R2, R3			10Ω, 5%, 1/4W, C.F.
R4	BC Components	CR25-22¬5%	22Ω, 5%, 1/4W, C.F.
R5, R6			7.5Ω, 5%, 1W, C.F.
R7			62Ω, 5%, 1/2W, C.F.
R8	BC Components	CR25-10K5%	10kΩ, 1/4W, 5%, C.F.
T1			Converter Transformer, XIC-002A

FRONT END

CODE	MFG	PART NUMBER	DESCRIPTION
F101			Fuse Wickman Series 19189, 3.5A Time Delay
TH101			NTC Thermistor, Keystone CL-160
MOV101			Varistor, 375VAC Panasonic EZR-V07D431
L101			Common Mode Choke, per dwg. XIC-003
L102			Common Mode Choke, 1.0mH/3.2A Coilcraft P3215-A
C101	Panasonic	ECQ-U2A224MV	.22µF, 250VAC, X-Capacitor
C102	Panasonic	ECQ-U2A224MV	.22µF, 250VAC, X-Capacitor
C103, C104	Panasonic	ECQ-U2A103MF	.01µF/250 VAC, Y-Capacitor
CR101, CR104	General Semi.	KBL08	Bridge Rectifier, 4A/800 PIV
C105 - C108	Panasonic	EEU-EB-2W220	220µF, 200V
R101	BC Component	CR25-220K5%	220kΩ, 5%, 1/4W, C.F.
R102	BC Component	CR25-220K5%	220kΩ, 5%, 1/4W, C.F.
R103	BC Component	CR25-4.7¬5%	4.7Ω, 1/4W, C.F.
S101	C&K	1101-M2-S3-C-Q-E	Switch SPDT

SECONDARY CONTROL

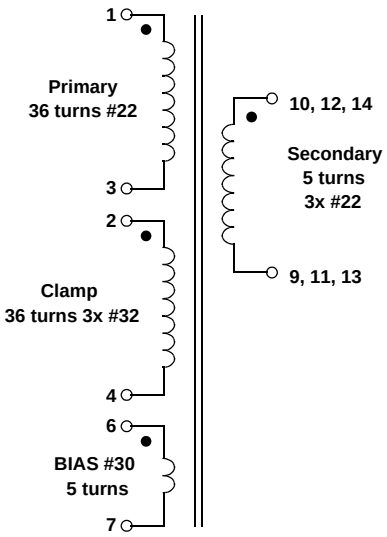
CODE	MFG	PART NUMBER	DESCRIPTION
C201			1000pF ±20%, 100V, X7R Ceramic
C202			0.1µF ±20%, 50V, X7R Ceramic
U201	Intersil	X9315	Digitally Controlled Potentiometer,10kΩ
U202, U203	MOT, TIS, PHA, SGS	TL431ACLP, T092	Programmable Reference
U204	INF, MOT, QUA	CNY17-2ZQT	Opto Coupler
R201	BC Components	CR25-1K5%	1kΩ, 5%, 1/4W, C.F.
R202	BC Components	CR25-2.7K5%	2.7kΩ, 5%, 1/4W, C.F.
R203	Dale	RN55C9531F	9.53kΩ, 1%, 1/4W, M.F.
R204	Dale	RN55C4402F	40.2kΩ, 1%, 1/4W, M.F.
R205, 206, 207, 208	Dale	RN55C2491F	2.49kΩ, 1%, 1/4W, M.F
R209	Dale	CR25-1K5%	1kΩ, 5%, 1/4W, C.F.
R210, 211, 212	BC Components	CR25-47K5%	47kΩ, 5%, 1/4W, C.F.

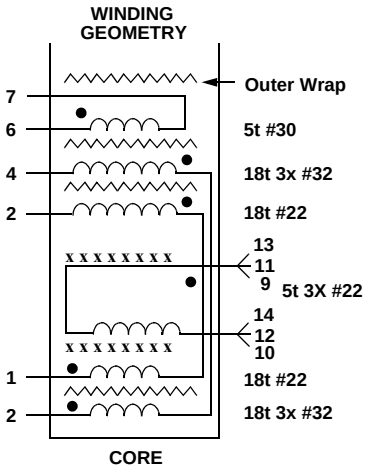
PRIMARY CONTROL

CODE	MFG	PART NUMBER	DESCRIPTION
U301	TIS, MOT, SGS	UC3844A	PWM Controller
U302, U303	Intersil	X9315	Digitally Controlled Potentiometer,10kΩ
C301	AVX	SR151C271MAA	270pF, 10%, 100V, X7R
C302	Panasonic	EEU-FCIE470	47µF, 25V
C303	AVX	SR205E104MAA	0.1µF, 10%, 100V, Z5U
C304	Dale	199D335X0016AA1	Tantulum, 3.3µF, 20%, 16V
	Kemet	T350A335J016AS	Tantulum, 3.3µF, 20%, 16V
	AVX	TAP335M016CRS	Tantulum, 3.3µF, 20%, 16V
C305	AVX	SR155A102KAA	1000pF, 10%, 50V, NPO
C306	AVX	SR155A101JAA	100pF, 10%, 50V, NPO
C307	AVX	SR215A471JAA	470pF, 50V, NPO, 10%
C308	AVX	SR155A102FAA	1000pF, 10%, 50V, NPO
CR301, CR302	MOT	MUR120	1A, 200V, Ultra Fast
L301			Inductor, 5mH, XIC-006
R301	BC Components	CR25-150¬5%	150Ω, 5%, 1/4W, C.F.
R302	BC Components	CR25-4.7k5%	4.7kΩ, 5%, 1/4W, C.F.
R303	BC Components	CR25-10k5%	10kΩ, 5%, 1/4W, C.F.
R304	BC Components	CR25-15k5%	15kΩ, 5%, 1/4W, C.F.
R305, R306			180kΩ, 5%, 1/2W, C.F.
R307	BC Components	CR25-330¬5%	330Ω, 5%, 1/4W, C.F.
R308	Dale	RN55C3321F	3.32kΩ, 1%, 1/4W, M.F
R309, R318			40.2kΩ, 1%, 1/4W, M.F.
R310	Dale	RN55C6491F	6.49kΩ, 1%, 1/4W, M.F.
R311-316	BC Components	CR25-47k5%	47kΩ, 5%, 1/4W, C.F
R317	BC Components	CR25-220¬5%	220Ω, 5%, 1/4W, C.F.
T1			Part of XIC-002A used on Power Mesh

Power Supply Magnetics

Converter Transformer XIC-002A





WINDING NOTES:

1. **All winding margins 3.2mm min.**
2. **All insulation full bobbin width**
3. **= operating insulation**
4. **x x x x x x x x= isolation barrier insulation (U.L.) double, .030" thick**

Core: Phillips ETD 34-3F3

Bobbin: Phillips PC1-34H

Wire: Heavy, class 130

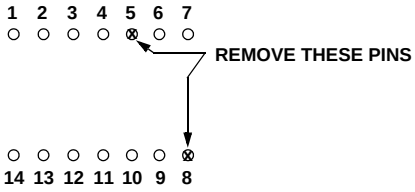
Primary Inductance: 3.0 mH ± 30% (no gap)

Hypot:

Primary to clamp	1000VDC
Primary to BIAS	2500VDC
Clamp to BIAS	2500VDC
Primary, clamp & BIAS to secondary & core	3750VAC per UL1950
Secondary to core	3750VAC per UL1950

Vacuum Varnish

All materials from same UL recognized class 130° insulation system



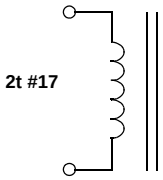
BOBBIN
(BOTTOM VIEW)

Available from:

Total Recoil Magnetics

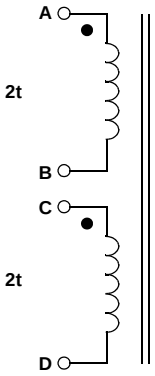
(508) 429-9600

High Frequency Inductor XIC-004



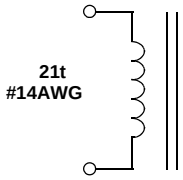
Core:	MICROMETALS	T26-26
Wire:	#17 heavy class	130°
Self Lead:	$^1/_2$" with $^1/_4$" tin	

Balance Inductor XIC-005



Core:	Phillips	89IT050
Wire:	#25 heavy	130°C
Leads:	self lead	$^1/_2$" with $^1/_4$" TIN
L_{A-B} =	2.3µH	±25%

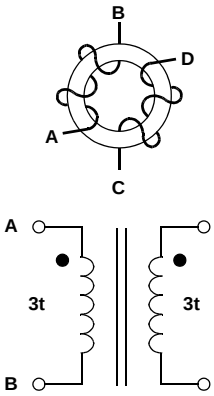
Power Supply Magnetics Output Inductor XIC-001



Core:	MICROMETALS	T106-18
Wire:	heavy class	130°C #14AWG, solderable
	L= 31mH ±15%	
Winding:	single layer	
Self Leads:	1" ± $^1/_4$", tinned last $^1/_2$"	

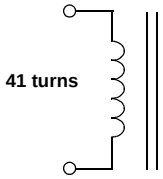
Available from:
Total Recoil Magnetics
(508) 429-9600

Common Mode Inductor XIC-003



Core:	**Phillips**	**T846T250**
LCM	**= 27.5µH ±25%**	
Wire:	**#20 AWG PVC 600V 105°C UL Style 1015**	

XIC-006 Inductor



Core:	**Phillips**	**204T250 3E2A Ferrite Torriod**
L =	**5µH ± 30%**	
Wire:	**Heavy class 130 #31AWG**	

A Simple XDCP Programmer

In the process of breadboard evaluation and debugging, the programmer provides a simple means to program the XDCP device. Figure 11 illustrates a simple programmer that was used to program the reference power supply design. The programmer is constructed with a 74C14 hex Schmitt trigger, three SPDT toggle switches and three 10K resistors. The 74C14 functions to de-bounce the switches such that the XDCP terminals have a clean level transitions. A step by step procedure for programming the XDCP device is given in Figure 11.

Programming the XDCP IC

1. Turn power off
2. Connect the programmer and set switches to:
   $\overline{CS}$
   U or D as desired
   $\overline{INC}$
3. Turn power on
4. Set programmer switch to CS
5. XDCP increments (decrements) when the switch is toggled from $\overline{INC}$ to INC. Repeat for each increment (decrement)
6. Using U/D & INC switches set XDCP Wiper to desired position
7. Set programmer switch to $\overline{CS}$ & $\overline{INC}$
8. Power Off
9. Disconnect programmer
10. When power is reapplied, the XDCP wiper position will return to its previously set position

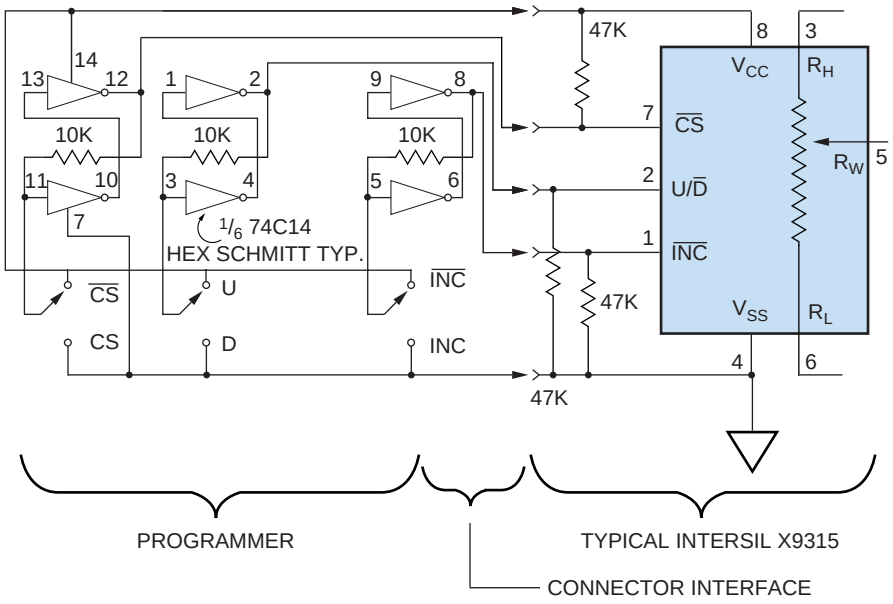


FIGURE 11. SIMPLE XDCP PROGRAMMER

Design and Construction Tips

With regard to the reference design:

1. To minimize common mode EMI, there must be a low inductance ground path from R103 ground (see Fig. 3) to output ground (see Fig.4). A copper tape with a width no less than one fifth of it's length is suggested.
2. Refer to Figure 4. The loop formed by T1 (pins 10, 12 and 14), CR5 anode, the junction of CR5 cathodes and through CR5 back to T1 (pins 9, 11 and 13) should be made as low an inductance as practical. This can be achieved by making the loop area physically small, using wide conductors and interleaving conductors where possible. Note that T1 the secondary pin out is staggered to allow interleaving.
3. The R/C snubber across each CR5 diode must be located physically close to the respective diode. Less than 1/2 inch is a good guideline.
4. The loop consisting of T1 primary (pins 1 and 3), Q2/Q3, Q1, R1, the negative side of C108/C107 (see Fig.3), the positive side of C105/C106 and back to T1 (pin1) on Figure 4 should be a low inductance loop.
5. C8 should be physically close to T1, (pins 3 and 4). A half inch is good. The same comment applies to C1 and T1, (pins 1 and 10, 12, 14).
6. Beyond the above, the usual power supply layout consideration should be followed, particularly with respect to grounding.

The Intersil X9315

1. Insure that the potentiometer (pins 3, 5 and 6) never are exposed to a voltage greater than Vcc or less than Vdd. This applies during dynamic conditions such as application of power.
2. Insure that the rate of rise of Vcc when power is applied is between 0.2V/ms and 50V/ms as specified in the Intersil X9315 data sheet.
3. To minimize the effect of temperature drift, use the potentiometer where the performance of the circuit depends on the ratiometric TC of the pot rather than the TC of the end to end resistance. The ratiometric temperature coefficient of the potentiometer is more than an order of magnitude better than the temperature coefficient of Rtotal as specified in the data sheet.